

WHAT IS CLAIMED IS:

1. An input/output port connector, comprising:
 - a storage element;
 - a probe in port;
 - a probe out port;
 - a data in port;
 - a data out port;
 - a scan in port; and
 - a scan out port;wherein, in a first mode of operation, contents of said storage element are used to select between data on said data in port and said probe in port to propagate directly to said probe out port.
2. A logic block, comprising:
 - a multiplicity of input/output (I/O) ports; and
 - a multiplicity of said input/output port connectors as in claim 1;wherein each of said I/O ports is connected to one of said multiplicity of block input/output port connectors; and wherein each said input/output port connector is connected to an adjacent one of said input/output port connectors by connecting said probe in ports of one input/output port connector to said probe out ports of an adjacent one of said input/output port connectors and said scan in ports of said one input/output port connector to said scan out ports of said adjacent one of said input/output port connectors, thus forming a string of input/output port connectors..
3. An integrated circuit comprising:
 - a multiplicity of logic blocks as in claim 2;
 - a multiplicity of bus connectors; and
 - a test bus;wherein each of said multiplicity of bus connectors is connected to said test bus, and wherein each of said strings of input/output port connectors is connected to one of said bus connectors.
4. An input/output port connector as in claim 1, wherein:

in a second mode of operation, data is propagated from said scan in port through said storage element to said scan out port,
in a third mode of operation, data propagates from said storage element to said data out port,
in a fourth mode of operation, data from said data in port is captured in said storage element, and
in a fifth mode of operation, data propagates directly from said data in port to said data out port.

5. An integrated circuit comprising:
a multiplicity of logic blocks:
an on-chip logic analyzer with a multiplicity of input ports: and
a multiplicity of probe lines:
wherein each of said probe lines is adapted to capture signals from said logic blocks and to propagate said signals to one of said multiplicity of input ports of said on-chip logic analyzer, said input ports of said on-chip logic analyzer comprising:
means to capture said signals from said probe lines:
means to align said signals propagated through said probe lines to create aligned signals: and
means to capture said aligned signals.
6. The integrated circuit as in claim 5, wherein said on-chip logic analyzer further comprises means to transfer said aligned signals out of said integrated circuit.